Solid State Relay Parallel and DC Operation (Appnote 61)

Description

Vishay Solid State Relay (SSR) outputs can be wired in parallel enabling the user to benefit from lower ON-resistance and higher load current for ac/dc switching applications. This technique is also useful to compensate for load current derating with increased ambient temperature, to minimize heat from output power dissipation, and for circuits that require redundancy. Also, many of Vishay SPST SSRs provide a center tap so that internal MOSFET switches can be paralleled for dc only switching applications.

Static Current Sharing

MOSFET switches operate as positive temperature coefficient resistors when VGS is large. The control circuit of Vishay SSRs supply ample gate bias to the MOSFET switches to ensure positive temperature coefficient R_{DS}on operation even with LED input currents as low as 2 mA. Therefore, with parallel MOSFET operation, if one MOSFET switch draws more than average current, its resistance will increase thereby counteracting the increased current. This intrinsic mechanism ensures that thermal equilibrium and stable current sharing is maintained.

To determine the maximum dc operating current from a set of paralleled SSRs, simply use the formula:

$$I_t = \sqrt{P_t / R_t} \qquad (1)$$

Where I_t is the maximum dc operating current for all paralleled SSRs; P_t is the sum of the power dissipation for all paralleled SSRs; and R_t is the parallel combination of all R_{ON}s for a given operating temperature.

Note:

- For ac/dc operation, SSR R_{ON} at high current can be less than the value stated in the Electrical Specifications section. This phenomena is due to a parasitic diode in the reverse conducting MOSFET. To take advantage of this lower R_{ON}, review the SSR's I-V characteristics, and then decrease the maximum electrical R_{ON} specification by approximately 10 %.

Observe the load current derating curves given in the Recommended Operating Conditions section of the appropriate data sheet and not to exceed 125 °C for T_j, where for a given SSR:

$$T_j = P_{thJA} + T_A \qquad (2)$$

Caveat

For operation at or near full rated current, if two SSRs in two different packages with identical R_{ON} electrical specifications are placed in parallel, one would expect the dc operating current to be double their rated load. R_{ON} is specified within a given range; if R_{ON} of the individual SSRs is not matched, one of the SSRs will draw more than half the current.

A better solution is to use a Vishay 2 Form A relay where the mismatch is minimal. These switches are fabricated on the same die, thereby providing optimum R_{ON} matching by virtue of the close proximity of one MOSFET switch to another. The single die construction also provides excellent thermal stability since all the switches now reside on the same paddle. Furthermore, R_{ON} matching is a specification on Vishay 2 Form A SSRs and is 100 % factory tested.

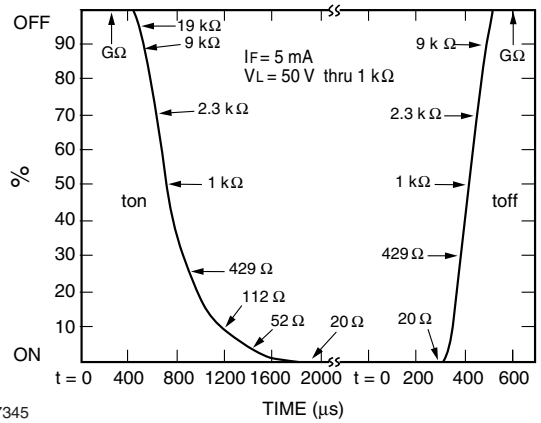

Figure 1. Dynamic switching resistance

Dynamic Current Sharing

Current sharing during switching is rarely a problem. Turn-on and turn-off times typically vary by a couple of hundred of microseconds for a given part number SSR. Switching slew rates are slow (~1 ms for t_{ON}), in effect keeping SSRs that are first to turn on in a high-impedance state until other paralleled SSRs have had time to turn on.

Figure 1 shows the typical dynamic switching resistance of the LH1500 SSR. If two LH1500 SSRs in parallel differed in turn-on time by 200 μs, when the faster LH1500 is fully on at 20 Ω, the slower LH1500 would have an ON-resistance of 36 Ω. Therefore, the faster SSR would have to source only 64 % of the load current for 200 μs. If the slew rates were fast, the faster SSR would have to source 100 % of the load current for 200 μs.

With different part number SSRs, turn-on time deltas can become more pronounced and here dissimilar turn-on times could momentarily subject the fastest

SSR to the full load current of the overall circuit. If many relays are paralleled to obtain a high-current operation, this current could potentially damage the SSRs. Most Vishay Form A SSRs employ integrated current-limiting circuitry that will protect the relay from high-current transient conditions. Dynamic current sharing can be ignored when current-limited SSRs are used. For SSRs without current limiting, be sure that the overall load current does not exceed the absolute maximum pulsed peak current specification of the respective SSRs.

dc Operation

Similarly, most of the 6-pin Vishay SSRs can be wired for dc only operation. In this configuration, pins 4 and 6 are usually tied together, thereby paralleling the two internal MOSFET switches. Pins 4 and 6 become the positive output of the SSR, and pin 5 becomes the negative output. Here too, the MOSFET switches reside on the same die and static and dynamic current sharing are not an issue.